# LAYOUT DESIGN ENGINEER

Antaios is a technology start-up, founded in 2017, developing SOT as the next generation of Magneto-resistive Non-Volatile Memory (MRAM).

As part of our development, we are now setting-up a design team for which we are looking for an Analog Layout Engineer.

## MISSIONS

You will take part in the drawing from the memory block level, bitcell and sense amps, up to the memory macro and test chip level, from implementation to verification.

In addition to layout, your mission also includes drafting technical specifications, design documents and procedure descriptions.

You will work closely with the process team to enhance together the memory device, and with the design engineers for accurate and efficient design. You may collaborate with other teams outside the company.

## PROFILE

You have a first experience in analog layout (preferably <28nm), you are curious about:

- Working closely to the technology.
- Toying with the design rules (for bitcell optimization).
- Juggling with EDA tools and PDK.
- Understanding analog blocks such as sense amplifiers, charge pump, and more generally how full integrated circuits work.

Experience in Non-Volatile Memory or Mixed Signal layout is a plus. You are interested to thrive in a fast-moving environment.

You are rigorous and disciplined in what you do and you will run the development processes under quality assurance.

You are autonomous, creative and reactive, and you are willing to be in position to make innovative proposals.

You have good communication skills and know how to work as a team.

You are fluent in English language, both speaking and writing, including technical vocabulary.

## CONTACT

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