CEA-LIST/DSCIN LFIM lab - Post-doctoral position

Non-volatile Asynchronous Magnetic RAM Design

Duration: 18 months

Beginning: October 2020

Project: NV-APROC, funded by the French ANR agency

Context

The Internet of Things (IoT) is one of the current main drivers for micro and nano electronics integrated circuit domain evolution. Strong constraints exist for IoT applications, especially in terms of power consumption and autonomy. The systems implementing such applications may have low activity ratio, leading to sleeping phases. Waking up from sleep is triggered by timer alarms, sensor events, RF events or energetic environment variations. In any case, a small part of the system has to remain active. Power consumption has thus to be optimized in all the circuit states, namely running, idle or sleep.

Data management while transitioning between these states is a new challenge. Moving data from a fast volatile memory to a non-volatile memory might take time and energy, leading to global performance reduction. Inserting non-volatility deeper in the system is thus crucial to enhance the quality of IoT solutions. In the frame of the project, we first propose to make the SRAM non-volatile by leveraging elementary non-volatile magnetic elements. Today efforts mainly focus on out-of-plane Spin Transfer Torque switching Magnetic Tunnel Junctions (STT-MTJ). However, according to the state of the art, a new generation of junctions, namely out-of-plane Spin Orbit Torque MTJ (SOT-MTJ), seems to be much more promising and interesting to evaluate.

Moreover, due to sporadic activity and event-driven activity in circuits, asynchronous logic implementation is a natural solution thanks to its robustness, its normally sleeping feature and its intrinsic event-driven operation. A Quasi Delay Insensitive (QDI) asynchronous processor will be developed in the frame of the project and will be associated with a non-volatile memory component. In order to ensure fast exchanges between the two entities and to avoid area overheads, the memory controller will also be built using asynchronous design techniques.

In this project, we will use an advanced Fully-Depleted Silicon On Insulator (FDSOI) 28nm technology process. Such a technology process is an interesting process candidate because it is advantageous in terms of energy, being fast and demonstrating low power consumption. In addition, in opposition to standard bulk processes, transistors substrate voltage may be controlled in a [-2V;2V] range in order to either reduce the static power consumption or improve the processing performance. These features may be leveraged to develop an efficient non-volatile asynchronous processor/memory couple.

Position

The position is available for a research engineer under a post-doctoral contract of 18 months starting in October 2020. The candidate will be integrated into the Advanced Mixed-Signal IC and Memory Design teams of the CEA-LIST institute. He will have close links with Spintec Spintronics IC design team and LIRMM laboratory, which both are collaborators of the project.

Mission

The main objective of this position is to develop a non-volatile asynchronous magnetic RAM component. To reach this goal, the candidate will first define a memory controller architecture suited for both asynchronous QDI components and non-volatility features. He or she will then develop a magnetic RAM component, all the way from RTL and schematic to layout, and validate it both throughout design and with the asynchronous processor. Finally, component will be characterized in terms of timing and power consumption to allow relevant system-level architecture exploration. An optional objective of the job is to study deeper integration of the non-volatility into the system, namely inside the standard cells.

All along this work, when opportunity arises, the candidate is expected to write scientific publications in order to highlight the innovative elements.

Education and skills

This position is available for candidates having a PhD diploma in electronics and willing to enhance their knowledge and skills in advanced topics such as memory design, non-volatility and asynchronous design. Existing knowledge and experience on these subjects would be appreciated.

Required skills:

- Spice, Cadence full-custom Design suite
- Verilog
- Simulation tools (ModelSim, eldo, ADMS, spectre)
- Layout
- Version control (git)
- Scientific papers writing

Contact

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