

Pôle CNFM de Limoges – PLM

CAO BF & RF et Dessin de layout (1 TP x 29 H)

Objectif : Etude d'un processus technologique CMOS, des transistors MOS en commutation, d'une méthodologie de conception de circuits simples CMOS. Dessin de layout et simulation.

Equipements/Logiciels : Stations de travail (SUN), Outils de CAO Cadence

Formation utilisatrice : Maîtrise E.E.A. - Faculté des Sciences et Techniques

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The screenshot displays the Affirma Analog Circuit Design Environment interface, which is divided into several windows:

- Top Left:** A control panel with tabs for Session, Setup, Analyses, Variables, Outputs, Simulation, Results, and Tools. It includes a Design table and an Analyses table.
- Top Right:** The Virtuoso Layout Editing window, showing a detailed layout of a circuit cell with various layers and components.
- Middle Left:** The Virtuoso Schematic Editing window, showing a circuit schematic with components like voltage sources (v1, v2) and a capacitor (C0).
- Middle Right:** A vertical toolbar containing various design tools and a list of layers such as NTUB, DIFF, PIMP, POLY1, NPLUS, PPLUS, POLY2, CONT, MET1, MET2, PAD, RESDEF, TUBRES, RESTRM, R0net, and DIFCUT.
- Bottom Right:** A Waveform Window displaying the Transient Response of the circuit. It shows three waveforms: VT("/Q"), VT("/B"), and VT("/A") over a time period from 0.0 to 6.0ms.
- Bottom Left:** A log window showing the loading of various files (simul.cxt, avv.cxt, spectre1.cxt, corners.cxt) and the current directory path.