

VHDL-AMS : behavioural modelling for hierarchical analogue design

Description

This course introduces the concept of hierarchical design of analogue circuits and VHDL-AMS circuit modelling. It is composed of a short lecture part and a major laboratory part where ADVanceMS software is used. A phase-locked-loop (PLL) has been taken as a design example. The scope of this course is to familiarise the behavioural modelling approach during the design phase of analogue circuits.

Contents

Introduction

- Why hierarchical design? Top-Down and Bottom-Up design.
- Why behavioural modelling?
- Why VHDL-AMS?

Language basics

- Syntax, circuit description.

Top-Down design

- Functional analysis and functional modelling
- Application to PLL.

Bottom-Up design

- Circuit analysis and behavioural modelling
- Application to PLL.

Discussion

- Comparison of description levels
- Software limitations
- Model library
- Design re-use

Audience

Students (DESS) and design engineers who have already designed analogue circuits at the transistor level and want to familiarise with behavioural modelling of analogue and mixed systems, using the standard VHDL-AMS.

Lecturers

Thomas ZIMMER, Noëlle MILET-LEWIS, Maîtres de Conférence, IXL Laboratory – Bordeaux 1 University

Course schedule

3 days

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