

L'industrie de la microélectronique et le SITELESC

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Conseil d'orientation du GIP CNFM
Saint Malo, 22 novembre 2010

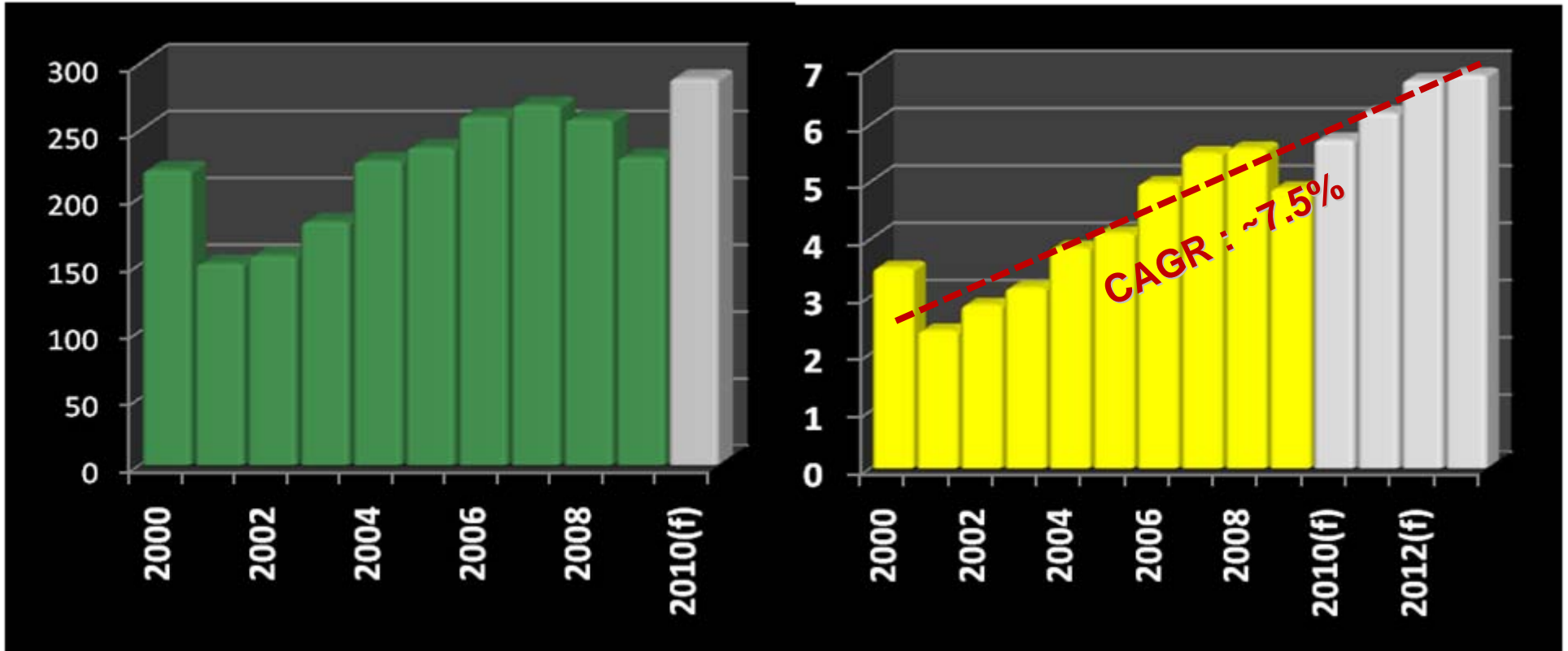


Back to Basics...

Semiconductors Market

Total Available Market (B\$)

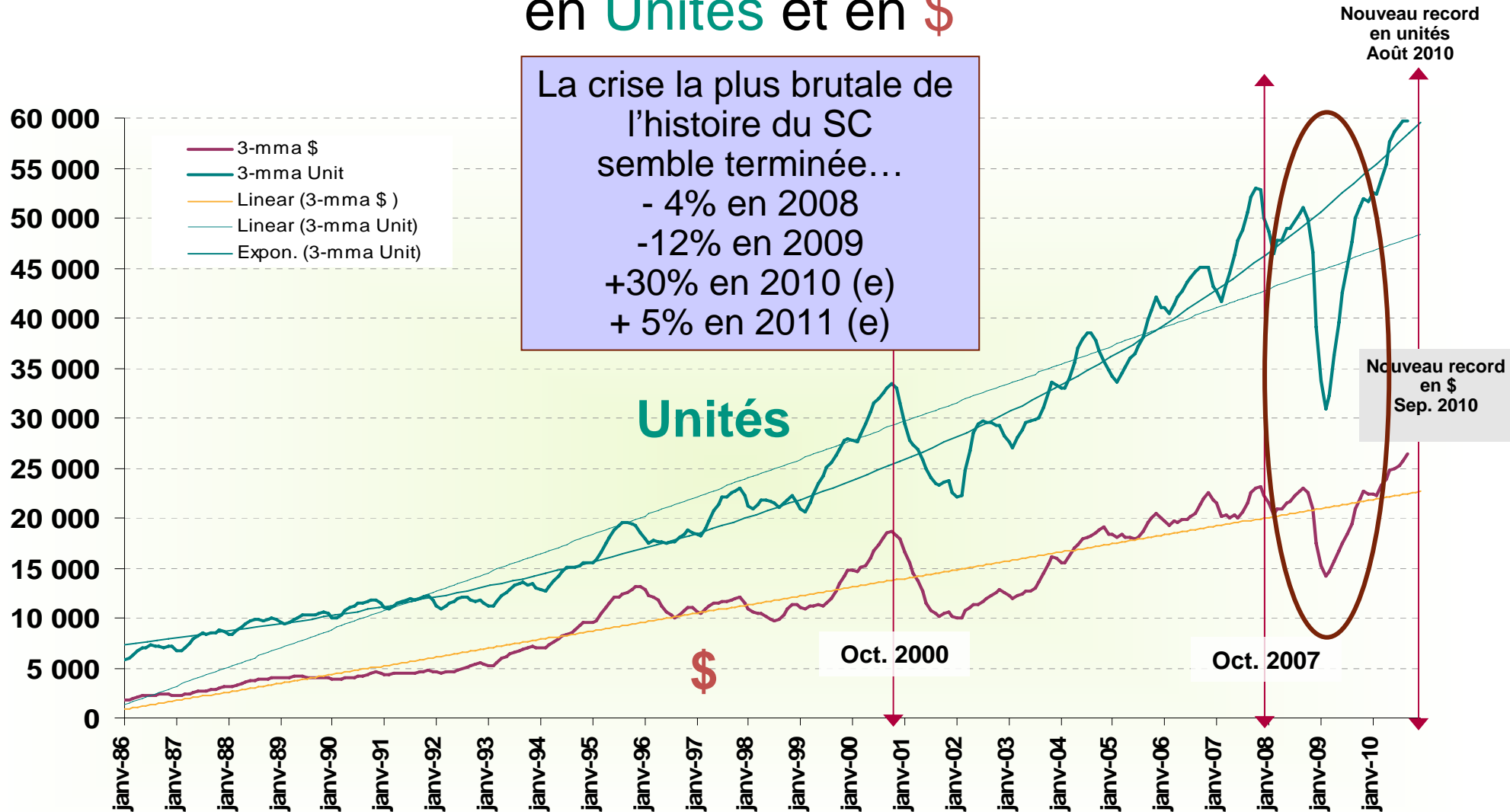
Total Area of Silicon Processed per Year (km²)



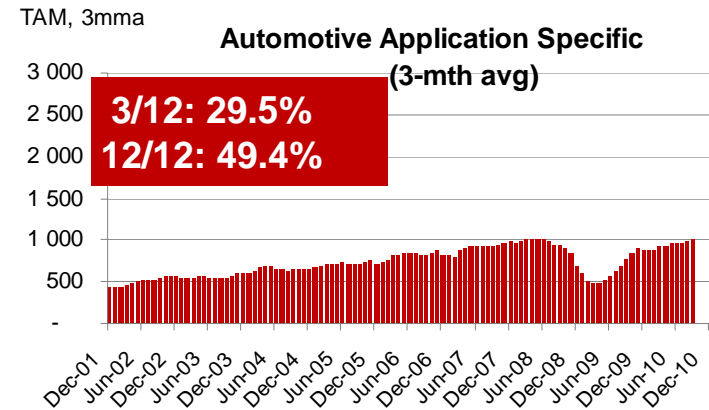
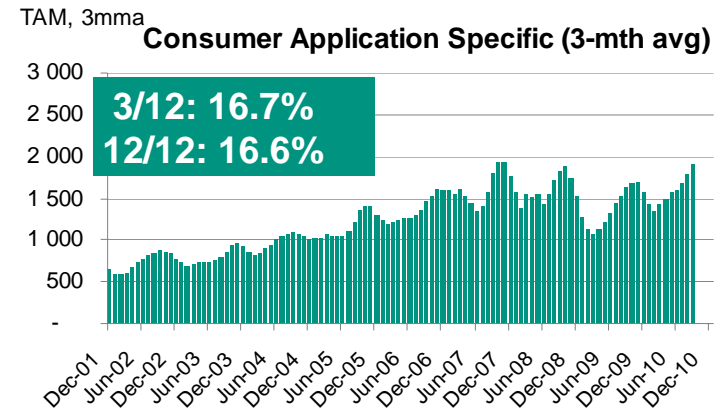
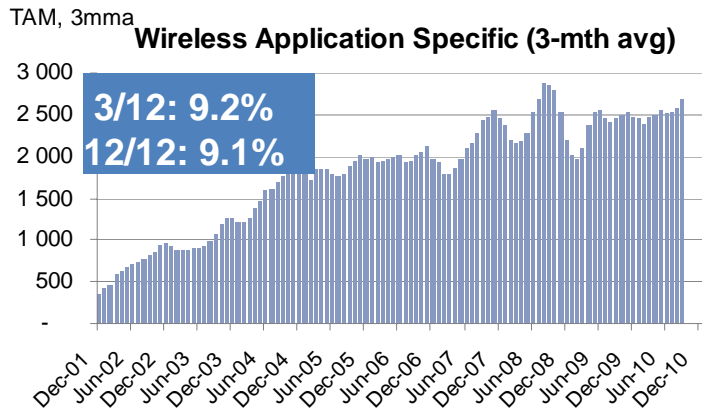
Source: ESIA, WSTS, ENIAC JU

Marché du Semiconducteur en 3-mma (sept 2010)

en Unités et en \$



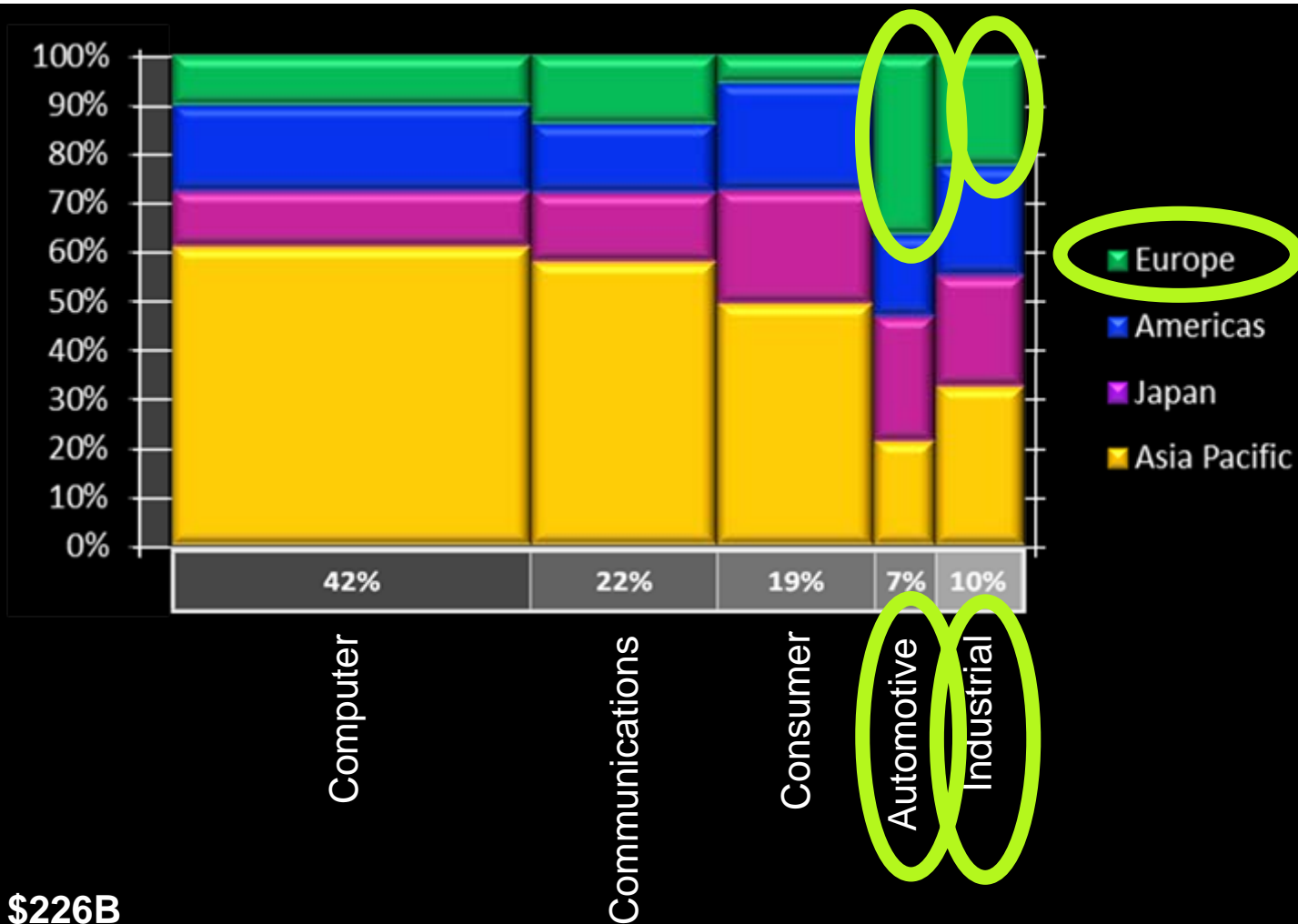
Cycle du marché par application à fin septembre 2010



Source : WSTS

Note : Application Specific IC's = MCU, DSP, Analog & Logic IC's by application

World SC Consumption (by billing/delivery address)

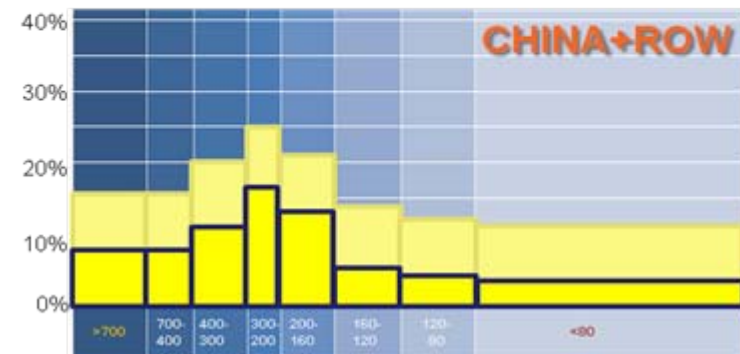
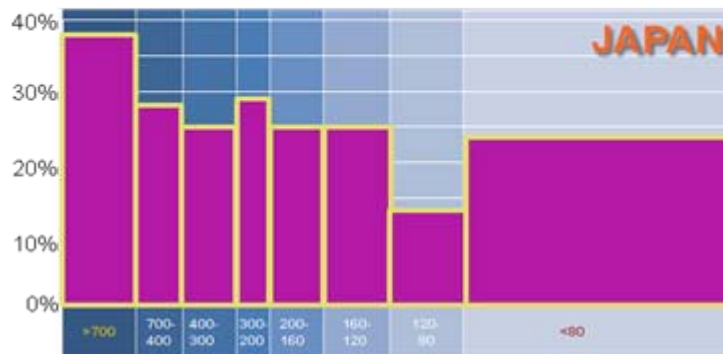
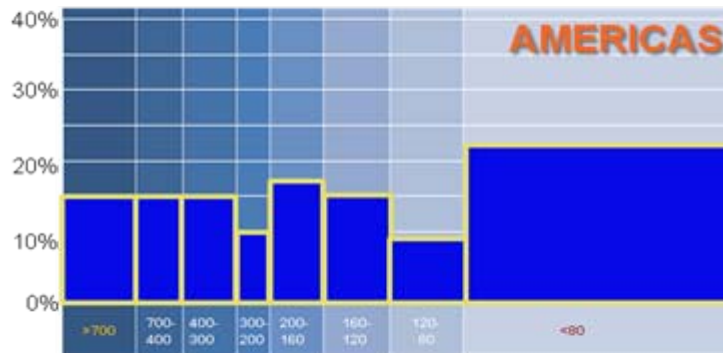
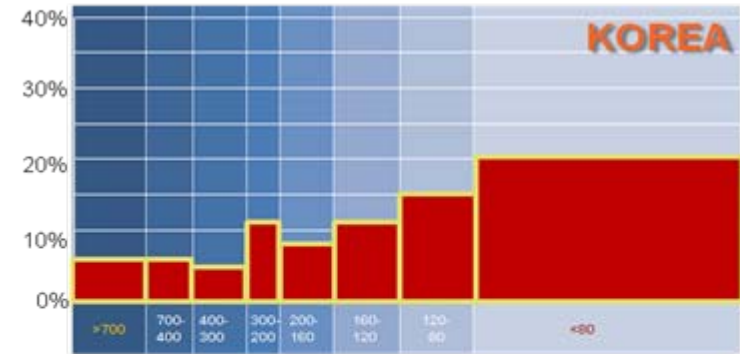
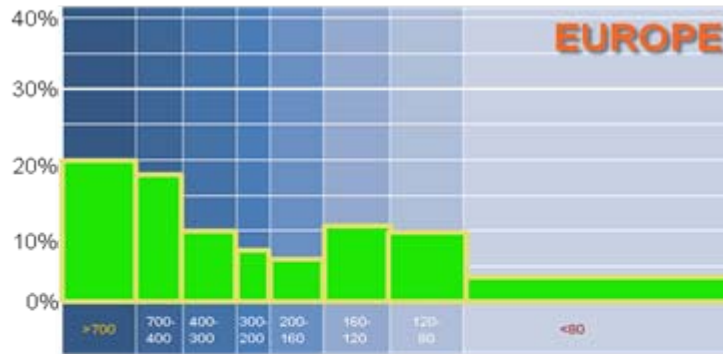


2009
World : \$226B
Europe : \$30B (13.3%)

Source: ESIA, ENIAC JU

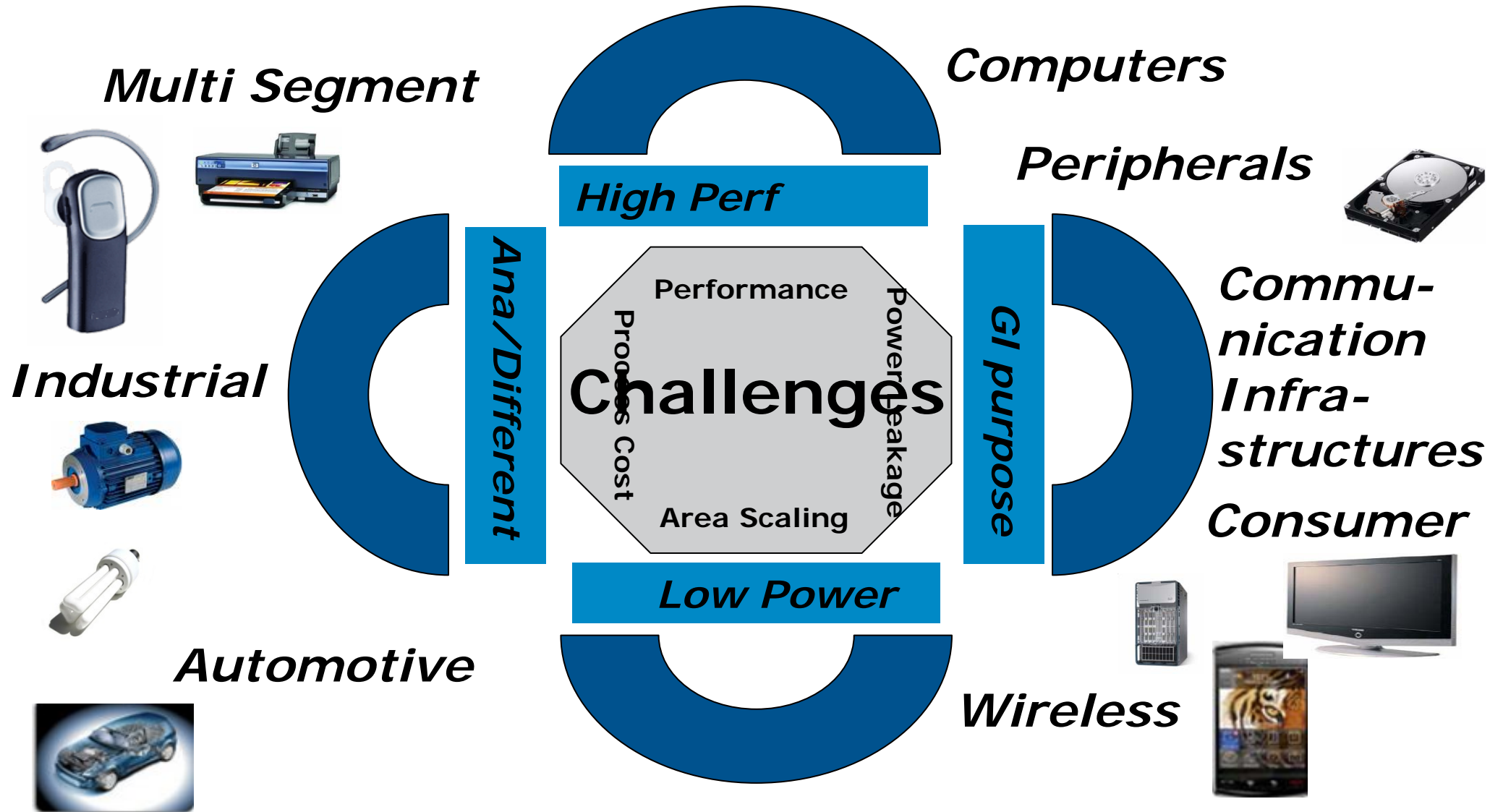
SC manufacturing Capacity: Japan, US and Taiwan lead, Europe Lags

Percentage of equivalent 200 mm wafers



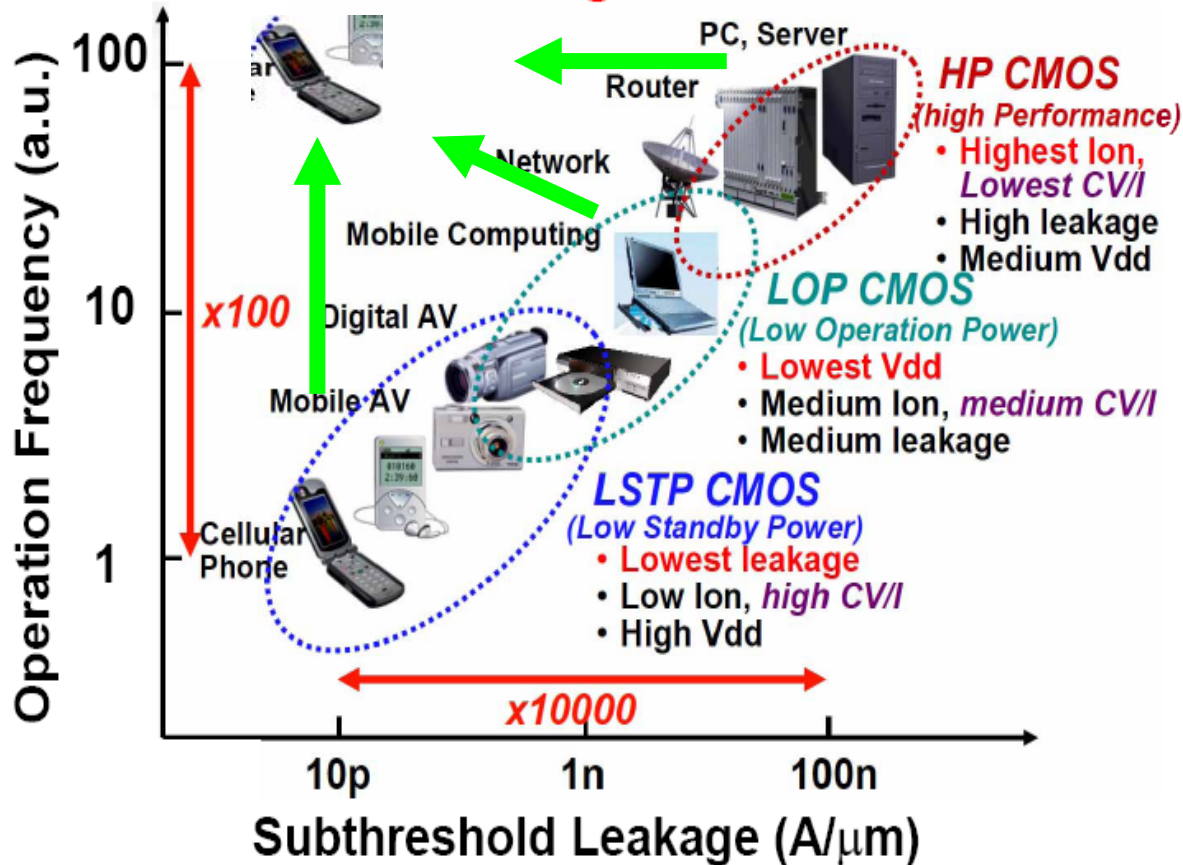
Source: IC Insights, ENIAC JU

CMOS Logic/Analogic Segmentation



Low Power Design Solution Needs

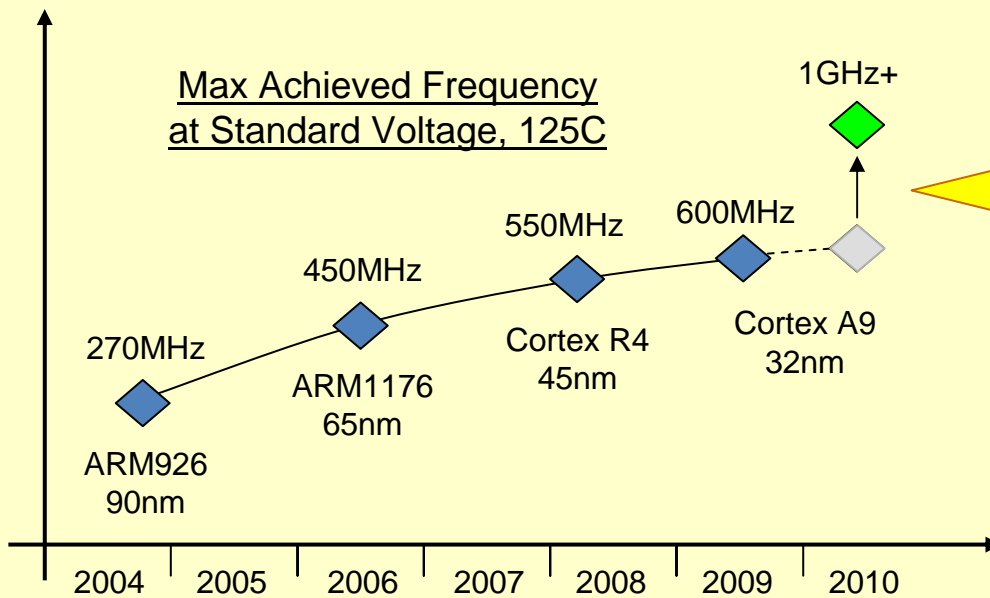
HP, LOP, LSTP for Logic CMOS



15

- Addressing 3 distinct product categories in 32nm
 - High End Wireless (1GHz/1W/100uW)
 - High End STB (1Ghz/4W/100mA)
 - High End Routers (1Ghz/70W/20W)
- Each requires dedicated solutions built with the following ingredients
 - Technology Variant
 - Library + IP
 - CAD Solution

Design: the GHz+ Implementation Challenge



Need to implement breakthrough techniques to step-up from natural evolution

Library tuning for best silicon behavior vs. design context tradeoff

Best metal routing pitch function of OPC transforms

Custom test solution with zero impact on design performance

Ad-hoc clock generator design to minimize sensitivity to process variations

Specific signoff margins based on actual implementation

...

- No single optimization area. Must implement global approaches.
- Strong co-optimization of Design/CAD/Process is key.

Advanced CMOS roadmaps convergence








65/55nm

45/40nm

32/28nm

22/20nm

High Performance




Bulk
SOI






General Purpose



















Low Power





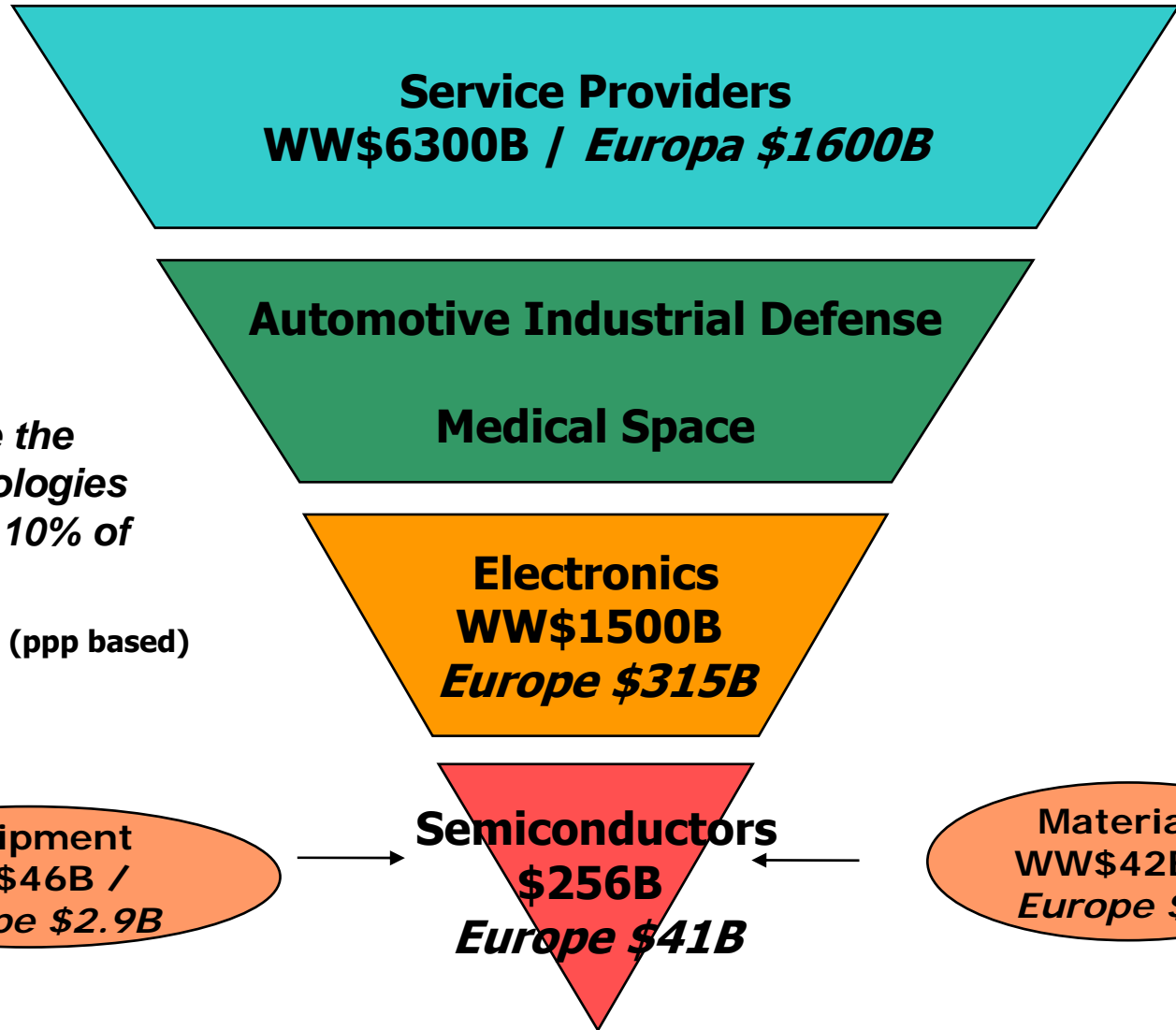









Semiconductors as key enabling industry



Semiconductors provide the knowledge & technologies that generate some 10% of global GDP.

2007 World GDP=65200BUS\$ (ppp based)

Micro & Nano-electronics: an opportunity for Europe

- Micro & Nano-electronics are impacting the **full European Value Chain** :
 - **30B€** contribution to Europe GDP
 - one of the few **Industries creating JOBS**
 - driving **90% of the INNOVATION**
 - positioning Europe as **WW leader in R&D**
 - **networking** WW leading Companies and numerous SME's
 - integrating R&D and Manufacturing within **CLUSTERS**
 - providing **SOCIETAL SOLUTIONS** via new technologies/applications
 - committing local, national and European **AUTHORITIES**

Therefore: Semiconductors, a KEY ENABLING TECHNOLOGY

Recommendations 2007 - 2009

SEMI

1. Develop a European vision for the industry
2. Increase funding for R&D and manufacturing
3. Promote the microelectronics supply chain
4. Cultivate education and welcome talent
5. Protect and enforce intellectual property
6. Involve SEMI Europe in new EHS legislation

EECA / ESIA

1. Reach agreement between the EU and Member States on priority segments
2. Lead market initiatives
3. Standardization and interoperability
4. Demonstration projects
5. Double the funding levels from €0.6bn to €1.5bn per year with 5 years
6. Revise rules on funding
7. Introduce or extend R&D tax credits
8. Reconsider the EU's state aid rules for semiconductor investments
9. Facilitate an EIB loan policy, allocation of up to €5bn

ZVEI / VDE Germany

1. Common European strategy for semiconductors (investment incentives, legislation for global competition)
2. Adjust rules of procurement for R&D in the German tax system (minimum taxation, loss carry forward)
4. Further development of PPP involving industry, academic research and public means
5. Investment-friendly ESH regulations
6. Consistent, efficient customs procedures

CALL FOR ACTION NOW!!

THE BASICS – *Four pillars*

Mastering Innovation

*Develop a European industrial innovation policy -
with nano- / microelectronics at its core*

R&D

Give priority to the European-wide micro- / nanoelectronics R&D in framework programmes, public-private partnerships (EUREKA, ETPs, JTIs), national programmes

Market pull

Stimulate 'market pull' across Europe in chosen lead markets
(Health and wellness; transport and mobility; security and safety; energy and environment; communication; infotainment)

Manufacturing

Launch a strategic European industry plan that aims at revitalising sc manufacturing capabilities in Europe. Upgrading /converting existing fabs. Developing technology capabilities for devices in areas where Europe has strengths.

Education

Make micro- and nanoelectronics in education an objective for filling the European talent pipeline:
Stimulate science and technology; awareness of the micro-/nano-electronics innovation potential; attract foreign talent; research infrastructure as invention incubators

Shaping the Future

LA REPRESENTATIVITE DU SITELESC

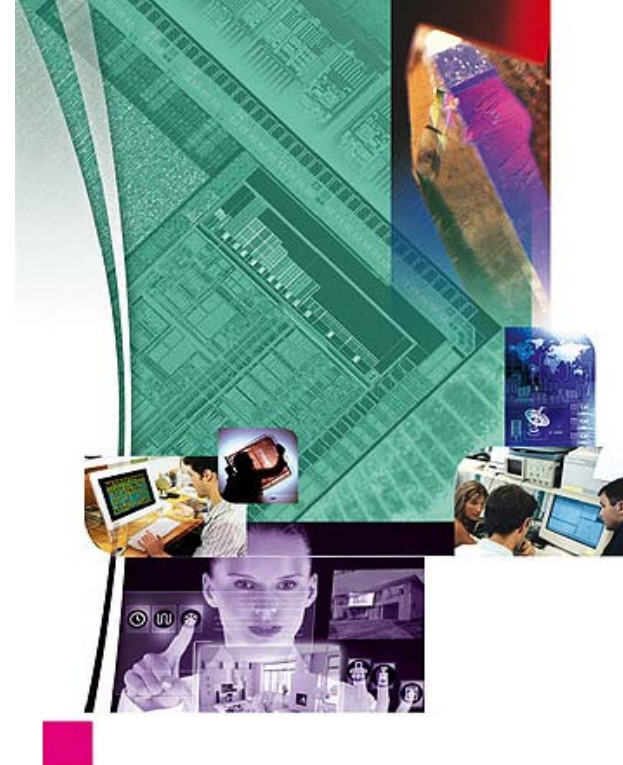
35 adhérents

35 sites industriels, R&D et Design

70 000 emplois directs et indirects

dt 18 000 ingénieurs et cadres

~ 4 milliards d'euros de CA





Les fabricants



Les laboratoires

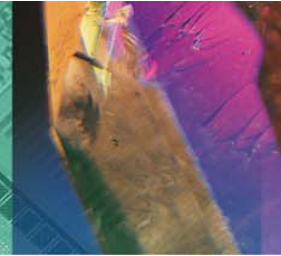
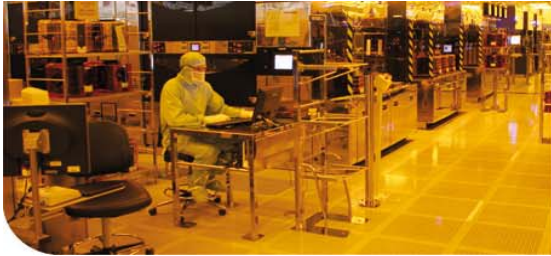


Les concepteurs

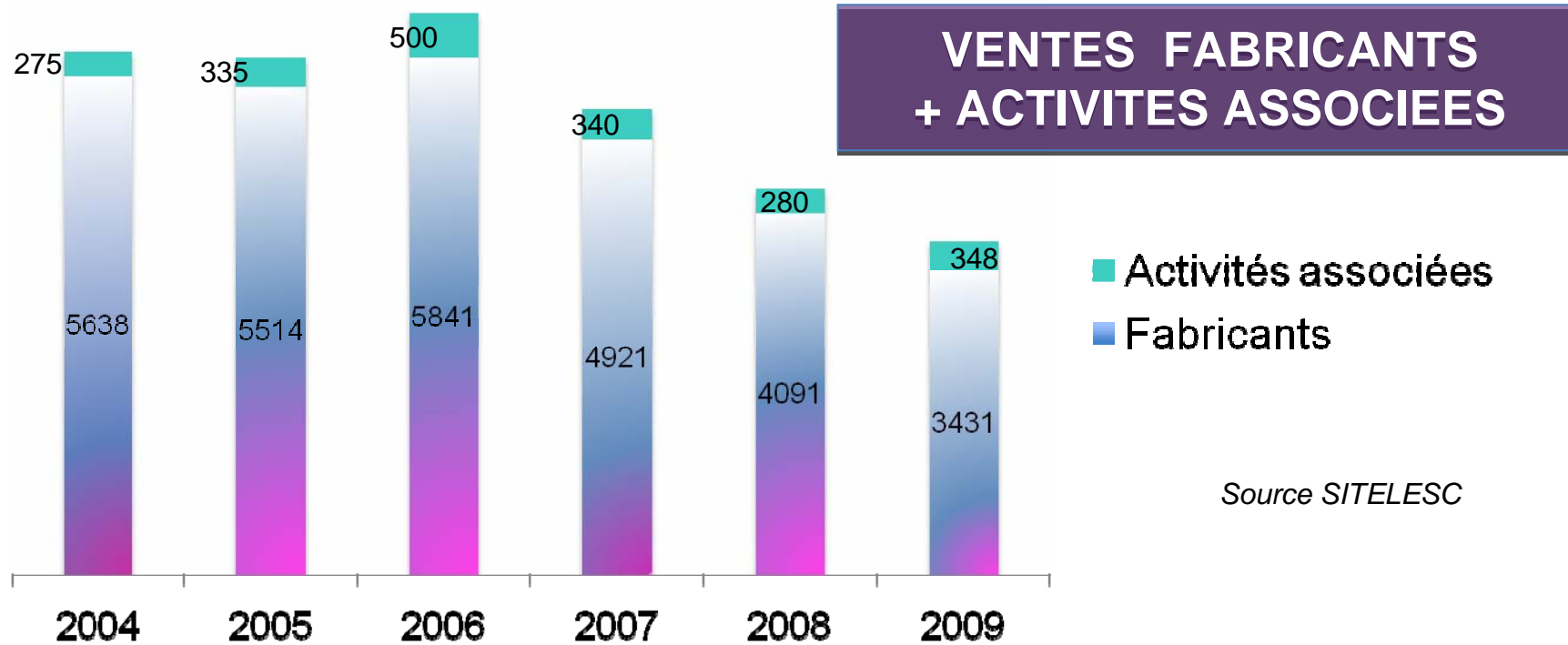


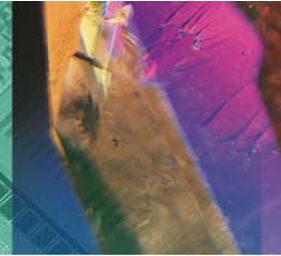
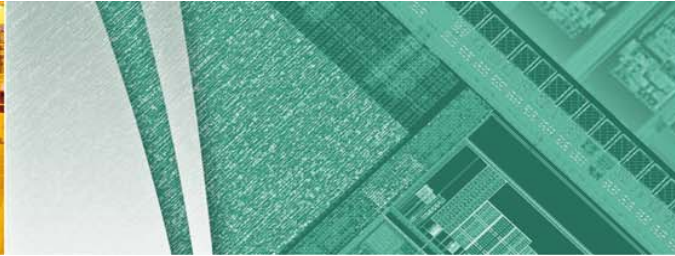
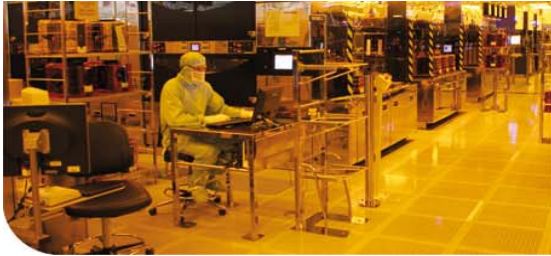
Les membres partenaires



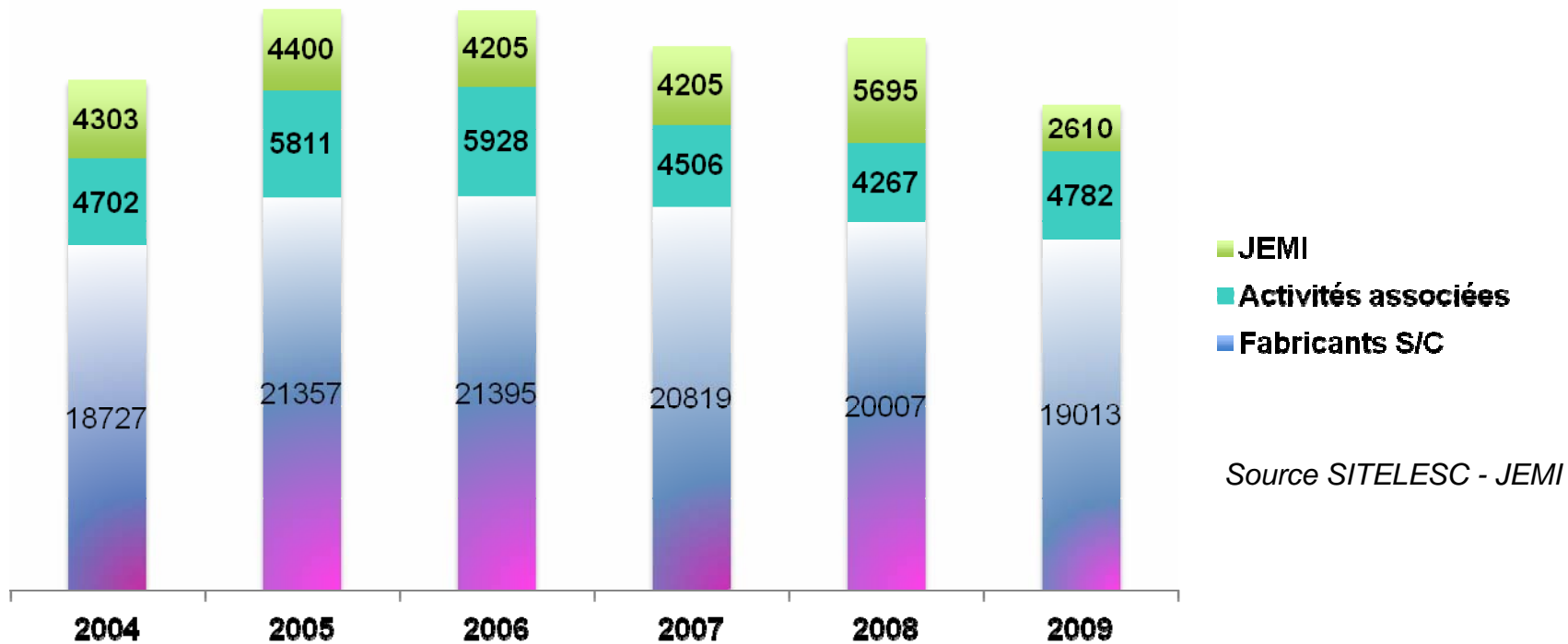


CA en M€





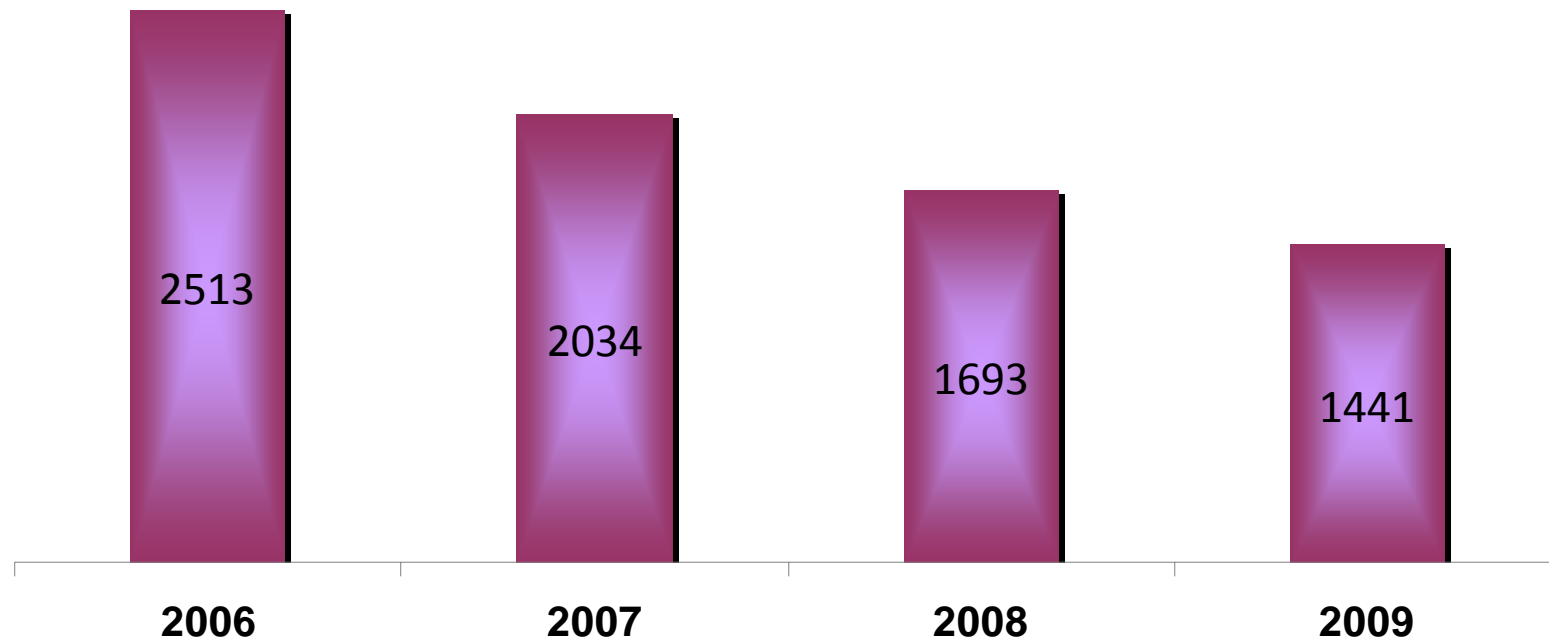
EFFECTIFS ADHERENTS



Source SITELESC - JEMI

MARCHE SEMICONDUCTEURS

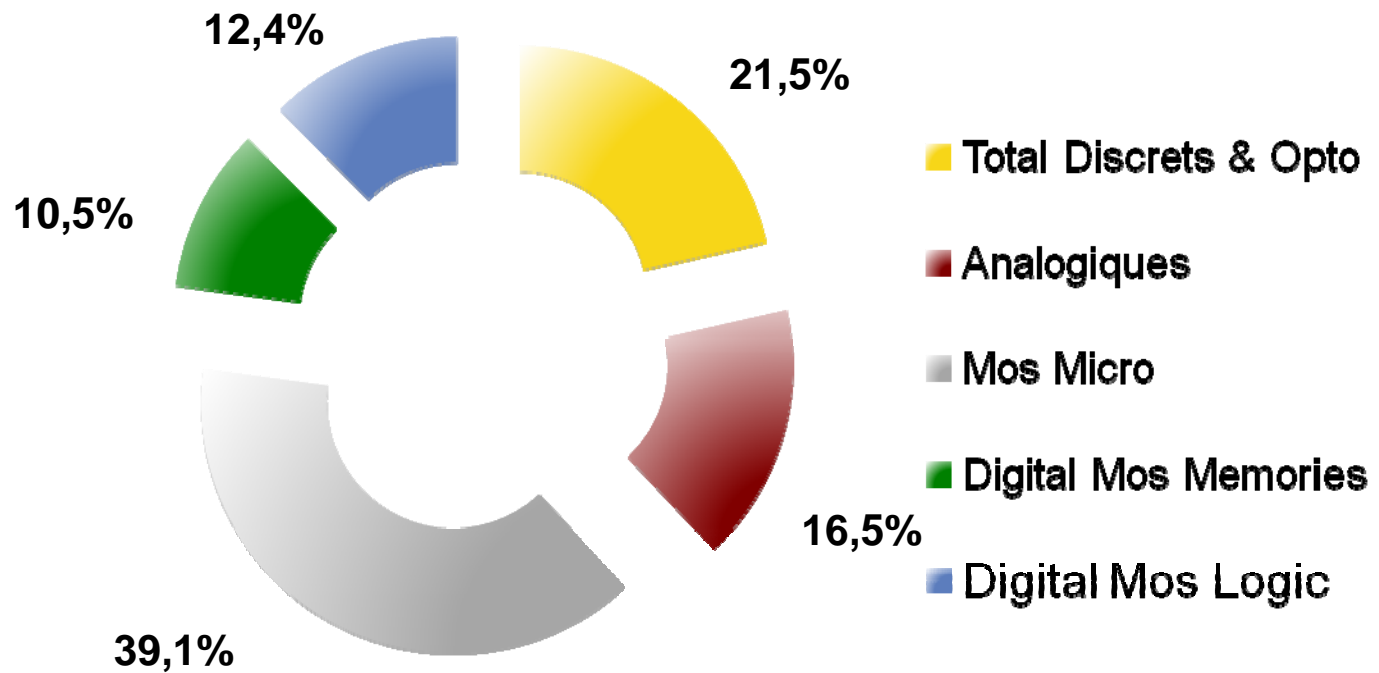
(Marché France en M€)



Source SITELESC - CLUBS

MARCHE SEMICONDUCTEURS

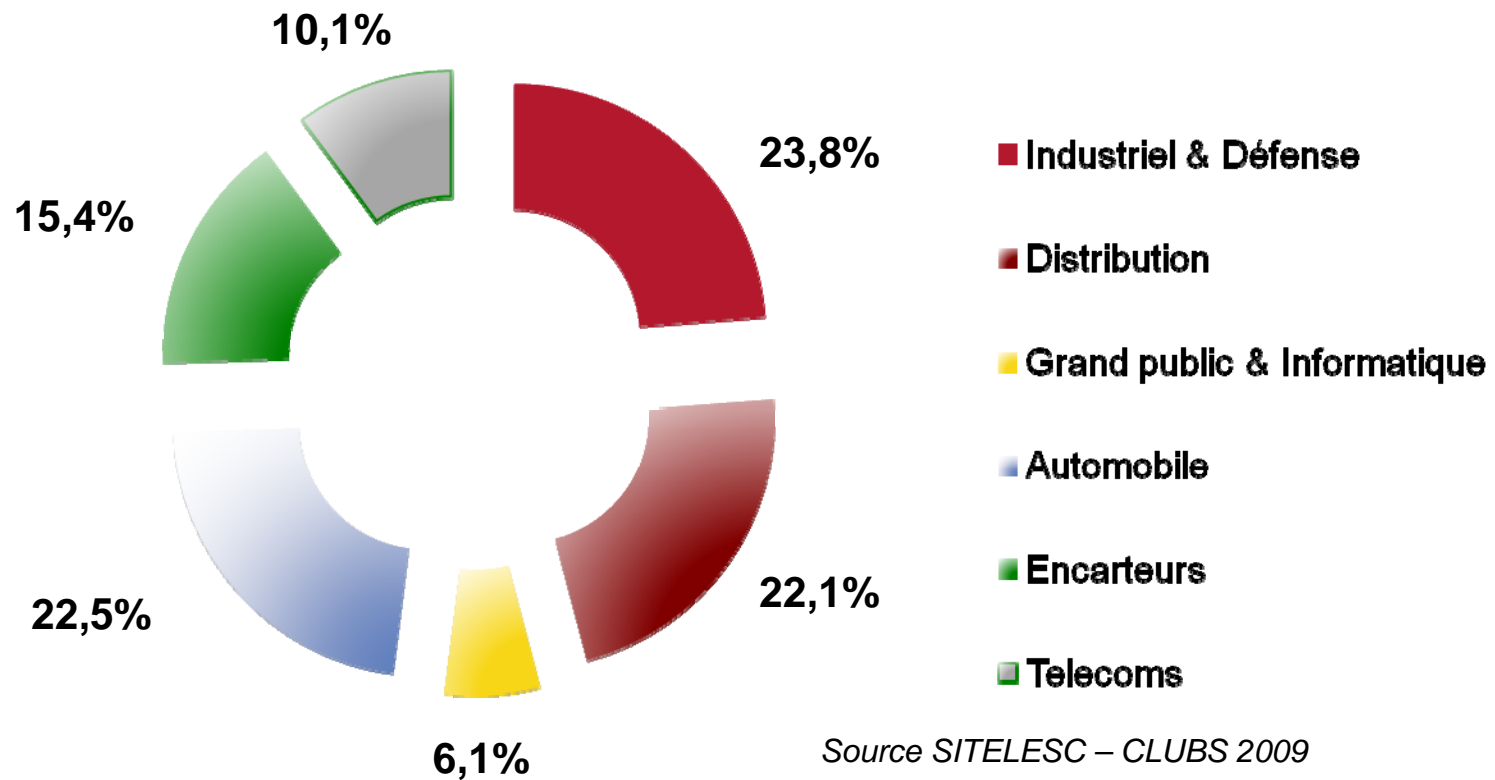
France, par familles de produits



Source SITELESC – CLUBS 2009

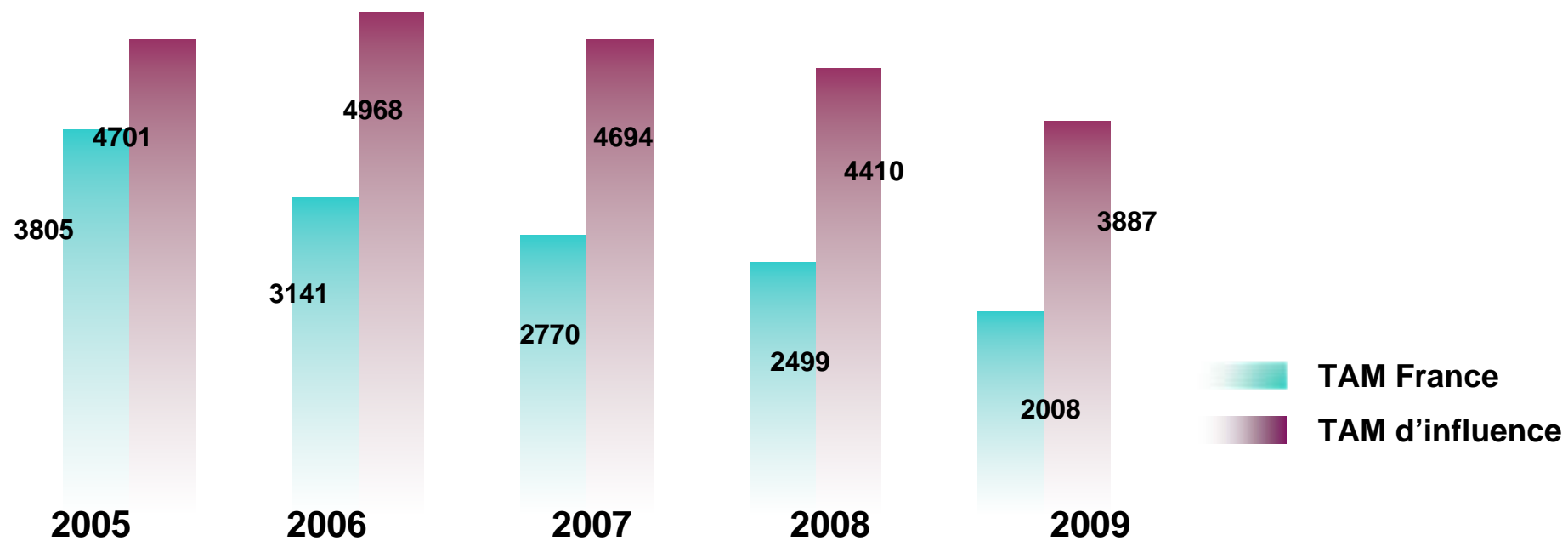
MARCHE SEMICONDUCTEURS

France, par domaines d'application



Source SITELESC – CLUBS 2009

TAM D'INFLUENCE (en M\$)



Source SITELESC - CLUBS

MISSION du SITELESC:

« Promouvoir, Défendre et Renforcer l'industrie du semi-conducteur en France et en Europe »

- **Actions Axe 1:** « Assurer la promotion de l'image de la profession et de son écosystème vers les autorités françaises, les filières de l'électronique, les universités, le public et les adhérents »

Comment: site web, newsletter, vidéo, actions filières, Communiqués de presse, conférence EMS, salon CIEN,.....

- **Actions Axe 2:** « Développer les synergies internes à la profession »

Comment: Commissions HSE, Economique, Affaires sociales, Clubs, lien avec l'ESIA,

- **Actions Axe 3:** « Offrir aux adhérents un support technique et assurer leur intégration dans le réseau des entités connexes »

Comment: Relais des informations FIEEC (juridique, économique, politique, sociale, technique), implication des adhérents dans les projets FIEEC de la filière électronique, CLEEE, guide CIR, Benchmarks,.....

- **Actions Axe 4:** « Adapter la formation des jeunes diplômés aux besoins des adhérents »

Comment: Support CNFM, Classe en entreprises, enquête métiers,.....