Growth, Characterization and Integration of Si/SiGe Heterostructures into TUNFETs

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Abstract:

Si/Si$_{1-x}$Ge$_x$ Heterostructured nanowires are grown by Reduced Pressure-Chemical Vapor Deposition (RP-CVD) using catalyst assisted Vapor Liquid Solid (VLS) and Vapor Solid Solid (VSS) method. We aim to obtain compositional (Si/Si$_{1-x}$Ge$_x$) and/or doped (p-i-n) heterostructures with abrupt interfaces. The resulting NW heterostructures are structurally characterized using e.g. transmission electron microscopy (TEM), X-Ray diffraction and confocal Raman microscopy so that the optimum synthesis parameters can be identified. Then, doping level is evaluated by four points contacts techniques and local probes measurements to study the dopants distribution. Kelvin Probe force microscopy (KPFM) and scanning capacitive microscopy (SCM) will be used for the characterization of dopant distribution. Further, these Nanowire structures are integrated to TFET applications, a detailed I-V characterization will be conducted on these devices in order to assess their performances in terms $I_{on}/I_{off}$ levels, subthreshold slope, and low frequency noise.

Introduction:

Straightforward downscaling of the metal-oxide-semiconductor field-effect transistor (MOSFET), the workhorse of the electronics industry, is on the verge of an end as nanoscale dimensions have been reached [1]. In order to reduce power dissipation of future integrated circuits (ICs), new device architectures and materials that support steep inverse subthreshold slopes and thereby low voltage operation are intensively investigated. A promising candidate to replace the MOSFET in future technology nodes is the vertical nanowire (NW) based tunnel-FET (TFET) [2]. Due to its built-in tunnel barrier, the TFET does not suffer from short-channel effects, and the subthreshold slope of TFETs is not limited to 60 mV/dec, the physical limit of MOSFETs. Moreover, the NW geometry offers the most ideal structure from an electrostatic perspective with 3-dimensional stacking capability. However, NWs also present other properties that make them attractive for advanced devices, such as the possibility of in-situ doping, core-shell structures, and the axial growth of non-lattice matched heterostructures. Axial NWs heterostructures allow energy band-edge engineering along the axis of the NW, which is the charge transport direction, and the realization of asymmetric devices for novel device architectures not easily accessible in planar devices. Interface abruptness of doped NWs and the heterojunctions in general imposes challenges in these structures and others for realizing high performance TFETs in p-i-n junctions or band gap engineered materials. In my work, we propose to investigate Si, SiGe, heterostructured nanowires (by varying the catalyst and growth parameters) as channel for TFET application.

Growth of Si/ Si$_{1-x}$Ge$_x$ Heterostructures by catalyst assisted VLS method using CVD:

Heterostructure formation in 1-dimensional (1D) nanostructures (nanowires) is important for their potential applications as efficient light emitting sources, better thermoelectrics, photonics, electronics etc [3-6]. Such Si/Si$_{1-x}$Ge$_x$ axial heterostructure nanowires are quite promising as components in the above mentioned areas because of smaller device dimensions and performance enhancements from quantum confinement [7-8]. These nanowires are fabricated via the vapor–liquid–solid (VLS) growth mechanism as shown by Wagner and Ellis [9]. This mechanism involves three main steps: Firstly, a metal particle absorbs semiconductor material and forms an alloy, this metal particle (catalyst) act as a site for the decomposition of precursors. In this step the volume of the particle increases and the particle often transitions from a solid to a liquid state. Secondly, the alloy particle absorbs more semiconductor material until it is saturated such that this saturated alloy droplet becomes in equilibrium with the solid phase of the semiconductor and nucleation occurs (i.e solute/solid phase transition). During the final phase, a steady state is formed in which a semiconductor crystal grows at the solid/liquid interface. The precipitated semiconductor material grows as a wire because it is energetically more favorable than extension of the solid-liquid interface. With the change in the precursors gases flow alternatively, the axial heterostructures can be obtained. Gold (Au) is a very commonly used catalyst for the growth of such structures but due to
the presence of the deep trap levels in the center of the bandgap, this metal is not microelectronics compatible. Moreover, the success of semiconductor integrated circuits has been largely hinged upon the capability of heterostructure formation through carefully controlled doping and interfacing. Therefore, in order to ameliorate and controlling the abruptness at the interface, it is assumed that there is a need of a catalyst which favours the growth by VSS Mechanism because in this method the phase of the catalyst remains solid and the growth occurs by the slow diffusion of adatoms. There are plethora of solid catalysts such as Ni [10], Pt [11], Ti [12], and many more which have been studied for the growth of Si NWs. Alexis [13] et al have shown that Palladium (Pd) as a solid catalyst can be promising for the growth of Nanowires by Silicide formation. Wu [14] et al have shown the formation of such structures using PE-CVD.

Characterization of interfaces of Si/\textit{Si}_{1-x}\textit{Ge}_{x} Heterostructures

In this work, we have shown the growth of Si/SiGe Nanowires using Au as catalyst. The Nanowires are grown in a CVD reactor at 450°C. The different segments and composition variation can be obtained by changing the precursors gases and their fluxes respectively. The abruptness attained is about 25 nm. The Nanowires have been characterized by various techniques such as SEM, TEM, EDS, Atom probe Tomography (in future work) in order to evaluate the diffusion length.
Characterization of Doping Content in the Nanowires

We will also make the study the doping concentration along the axis of Nanowire using Scanning Capacitive Microscopy (SCM). This technique has become the preferred technique for imaging dopant variations in semiconductor devices. Recently, Vallet [15] and coworkers have realized the axial doping along the axis of Si NW using SCM.

![Fig4](image1)

**Fig4:** (a) TEM image of a 90 nm diameter Si nanowire oxidized at 800 °C for 15 min, resulting in a SiO2 shell that is 4 nm thick. The wire is single crystal along its entire length. (b) SCM measurement of a thermally oxidized p-n+ Si nanowire, showing dC/dV contrast. Bright areas correspond to p-type doping, while dark areas are n-type. The intensity is related to the magnitude of dC/dV. (c) Line scan of dC/dV determined by averaging across the width of the Si nanowire. The metallurgical junction is present where dC/dV = 0. The thermally oxidized nanowire has a graded p-region and an abrupt n-n+ junction.

The above shown SCM results indicates that even though the p- and n-type dopant gas sources were switched abruptly during VLS, a p-n-n+ doping profile was obtained hence, confirming p-n junction along the axis of the Si nanowire following their thermal oxidation.

Further, the doping distribution will be studied by Atom probe Tomography.

Integration of Si or SiGe Nanowires into devices

Rosaz [16] et al have already shown the integration of Vertical Si and SiGe Nanowires into Planar and Vertical FETs. They have shown that vertical devices using Si NWs exhibit good characteristics with Ion/Ioff ratio close to 10^6 and sub-threshold slope around 125 mV/decade whereas vertical SiGe devices obtained with the same technological processes present a satisfactory Ion/Ioff ratio from 10^5 to 10^6 shown in Fig6. This comparatively low dynamics as Si Vertical FETs was explained by the high interface traps density.

![Fig5](image2)

**Fig5:** (a) Forty-five degree tilted SEM image of a wrap gated Si1-xGe_x nanowire. The gate length is around 200 nm (b) Forty-five degree tilted SEM picture of the top of an oxidized SiGe nanowire before the top contact realization. We can clearly see the oxide shell whose thickness is around 25nm. (c) Schematic of the SiGe NW based vertical transistor.

![Fig6](image3)

**Fig6:** (a) Typical output characteristic of a SiGe nanowire based vertical transistor for various gate voltages with VDS varying from 0.5 to 0.5 V (b) I_D-S–V_G_S characteristics at various drain-source voltages. The inset shows the threshold voltage value around 3.9V.

Conclusions:

We have demonstrated the realization of Si/ Si1-xGe_x Axial Heterostructures by RP-CVD using VLS and VSS methods. We have also shown the possibility of in-situ doping and controlling the abruptness in these structures as well as precise characterization of them. These structures have enormous capability to act as conduction channel in the transistor as the design of such HS will enable to go below sub-threshold slope i.e 60mV/decade, which is a big challenge.

References:


