UTBB FD-SOI: The Technology for Extreme Power Efficient SOCs

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Technology R&D
Bulk transistor is reaching its limits

Limited body bias capability

Complex channel architecture

Heavily Doped Wells

Fully Depleted devices are mandatory to continue the technology roadmap

FD-SOI = 2D

FinFET = 3D
28nm Planar UTBB FD-SOI Transistor

36 Masks:
7ML
Dual Vt - Dual Oxide

Thin Body (7nm)

Ultra Thin Body & BOX Fully Depleted SOI transistor
28nm Planar UTBB FD-SOI Advantages

- Shorter channel length
  - 24nm technology!

- Better electrostatics
  - Faster operation
  - Low voltage
  - Reduced variability

- Total dielectric isolation
  - Latch up immunity

- Lower leakage current
  - Less sensitive to temperature
28nm FD-SOI is same cost as 28LP, same performances as “G” technologies

FD-SOI, the only technology allowing the continuation of the Moore’s law

Source: ST/Marketing 2013, IBS 2013
FD-SOI: the best solution to 10nm

<table>
<thead>
<tr>
<th>Year</th>
<th>2012</th>
<th>2013</th>
<th>2014</th>
<th>2015</th>
<th>2016</th>
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<tbody>
<tr>
<td>28nm FD-SOI</td>
<td><strong>AVAILABLE TODAY!</strong></td>
<td></td>
<td><strong>TODAY IN DEVELOPMENT</strong></td>
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<td><strong>TODAY IN R&amp;D</strong></td>
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<td>14nm FD-SOI</td>
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<td>10nm FD-SOI</td>
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Advantages of FD-SOI:

- **28nm FD-SOI**
  - 0.9V
  - 113CPP
  - 90Mx
  - +30% speed
  - -30% power
  - (at same speed)

- **14nm FD-SOI**
  - 0.8V
  - 90CPP
  - 64Mx
  - +20% speed
  - -25% power
  - (at same speed)

- **10nm FD-SOI**
  - 0.7V
  - 64CPP
  - 48Mx

CPP: Contact to Poly Pitch
Mx: Pitch at Metal layer
### FD-SOI Benefits vs. Other Technologies

<table>
<thead>
<tr>
<th></th>
<th>Bulk</th>
<th>FD-SOI</th>
<th>FD-SOI</th>
<th>FinFET</th>
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<tbody>
<tr>
<td></td>
<td>28 LP</td>
<td>28 G mobile</td>
<td>28FD</td>
<td>14FD</td>
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<td><strong>Power Efficiency</strong></td>
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<tr>
<td>in high performance mode</td>
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<tr>
<td>Power Efficiency in low power mode</td>
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<td><strong>Extended DVFS</strong></td>
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<tr>
<td><strong>ULV capability</strong></td>
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<tr>
<td><strong>Cost</strong></td>
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<td><strong>Process Simplicity</strong></td>
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<td><strong>SER immunity</strong></td>
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<td><strong>Heat dissipation</strong></td>
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<td><strong>Analog Performance</strong></td>
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### Conclusion:
- 28FD consistently better than any 28nm alternative
- 20nm irrelevant for many segments: better use 28FD or go to 14FD
- 14FD consistently better than 14/FF
UTBB FD-SOI Design EcoSystem

• FD-SOI uses a conventional bulk design flow
  • Cadence, Mentor, Synopsys,
  • Apache, Atrenta

• 4-terminals spice models available, from PSP
  • Major simulators supported

• UTBB FD-SOI uses same low power design techniques than for bulk. In addition:
  • Optimized power switches
  • Extended poly-bias
  • Reverse & forward Dynamic body bias
Body Biasing (BB)

A very reasonable effort for extremely worthwhile benefits

- An extremely powerful and flexible concept in FD-SOI to:
  - Boost performance
  - Optimize passive and dynamic power consumption
  - Cancel out process variations and extract optimal behavior from all parts

- Comparatively easy to implement – if you’ve ever done DVFS you’ll have no difficulty with Body Biasing
  - No area penalty compared to Bulk
  - Reuse of Bulk design techniques
  - Speed/Power control

Back-gate contact
Extended Body Bias Range in UTBB FD-SOI

Efficient knob for speed/leakage optimization

BULK

UTBB FD-SOI

-300mV  +300mV

-3V  +3V

Efficient knob for speed/leakage optimization
Body Bias Efficiency - Silicon Benchmark

**Frequency (MHz)**

- **no BB**: REF
- **FBB 1V**: +20%
- **FBB 2V**: +40%
- **FBB 3V**: +60%

**Leakage (pA)**

- **0.5V**: REF
- **1V**: /7
- **1.3V**: /30
- **RBB**: /50
## FBB usage per market segment

<table>
<thead>
<tr>
<th>Market Segment</th>
<th>Infrastructure - Networking</th>
<th>Consumer</th>
<th>Internet of Things</th>
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</thead>
<tbody>
<tr>
<td><strong>Supply</strong></td>
<td>0.7 – 0.9V</td>
<td>0.6 – 1.1V</td>
<td>0.6V-0.9V</td>
</tr>
<tr>
<td><strong>Configuration</strong></td>
<td>high number multicore, DVFS &amp; FBB tuning for best MIPS/W ratio. Adapt perf &amp; power to workload</td>
<td>Wide DVFS, FBB linked to CPU workload &amp; thermal conditions</td>
<td>Ultra Low Voltage 0.3V-0.4V, FBB to solve the power/performane paradigm, Reverse Body Biasing</td>
</tr>
<tr>
<td><strong>Power efficiency</strong></td>
<td>28 FD-SOI: Up to -50% total power reduction versus 28G(mobile) @ 0.6V, FBB for ultimate power efficiency tuning</td>
<td>28 FD-SOI: Up to -50% power reduction, FBB provides +18% max. performance boost versus 28G(mobile)</td>
<td>28 FD-SOI: Up to x 4 perf/power ratio versus 28G(mobile) at low voltage, Low voltage power efficient performance. Reduce idle current</td>
</tr>
<tr>
<td><strong>Flexibility Perf/Power</strong></td>
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<tr>
<td><strong>Ultra power efficiency</strong></td>
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FD-SOI enabling Ultra-Wide DVFS

• FD-SOI allows the widest Vdd range for voltage scaling

• Still guaranteeing top notch speeds at very low operating voltage
  • >5x when compared to 28LP technology
  • >35% when compared to 28G technologies

Real measurements of continuous DVFS in the range 0.5V – 1.4V
Performed on a very large number of ICs, showing extremely good reliability of the DVFS in this range
28nm FD-SOI Best in class efficiency

@ high Vdd

@ low Vdd

+43% vs 28LP

+83% vs 28G

FD-SOI 28nm - +600mV FB6

+50% vs 28LP

+25% vs 28G

bulk 28nm G

bulk 28nm LP

Energy efficiency (relative DMIPS/mW)

Speed (relative DMIPS)

@ low Vdd

@ high Vdd (overdrive)
FD-SOI: Efficiency at all levels

**CPU, GPU and logic**
- FBB dynamic modulation to get the best total power
- Best dynamic power /leakage tradeoff

**Memories**
- Memory bit cells in FD-SOI have much less leakage compared to Bulk

**Analog & High-speed**
- FD-SOI analog performance far beyond Bulk one
- Better figure of merit than FinFET for high-speed IPs

- Extended body bias range
- Fully depleted channel
- Lower gate leakage
- Lower channel leakage

Better transistor electrostatics
FD-SOI
The best technology choice

Superior and flexible technology

- FD-SOI transistors are faster, cooler, simpler
- Outstanding power efficiency across all use cases
- Efficiency at all levels: CPU, logic, Memories, Analog
- Manufacturing infrastructure and process reuse
- Improved reliability

Enhanced design options

- Very large operating range for the same design
- Back-biasing as a flexible and powerful optimization
- Ultra-wide range DVFS
- Enhanced efficiency of multi-core processing
- Easier design than FinFET

Gives your SOC competitive advantages

- Costs: chip-level and/or system-level (e.g. cost of cooling)
- Thermal power dissipation (TDP)
- Extended battery life
- Computing Power / Speed / Reactivity
- Reliability
- Time-to-Market